

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of :  
: Group Art Unit: Unknown  
Rommel, et al. :  
: :  
Serial No.: Not yet assigned : Examiner: Unknown  
: :  
Filed: Herewith :  
: :  
Title: Method of Making A Semiconductor Device, and Semiconductor Device Made Thereby

**INFORMATION DISCLOSURE STATEMENT**

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir: :

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Title: Method of Making A Semiconductor Device, and Semiconductor Device Made Thereby  
Serial No.: Not Yet Assigned  
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authorized to charge any fee deficiency required by this paper or credit any overpayment to  
Deposit Account No. 02-4467.

Respectfully submitted,

Dated: March 10, 2004

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Thomas LeVance  
Printed Name: Thomas LeVance

FORM PTO- 1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.  0139376	SERIAL NO
INFORMATION DISCLOSURE STATEMENT BY APPLICANT  (Use several sheets if necessary)		APPLICANT Remmel, et al.	
		FILING DATE March 10, 2004	GROUP

## U.S. PATENT DOCUMENTS

EXAMINE R INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,500,724	12/31/02	Zurcher et al.			
	6,180,976	1/30/01	Roy			
	5,926,359	7/20/99	Greco et al.			
	5,731,747	3/24/98	Van De Walle, et al.			
	5,708,559	1/13/98	Brabazon, et al.			
	6,117,747	9/12/00	Shao, et al.			

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	2000228497	8/15/00	Japan			No	

## OTHER DOCUMENTS (Including Author, Title, Date Pertinent Pages, Etc.)

	Yoshitomi et al., <u>High Performance MIM Capacitor for RF BiCMOS/CMOS LSIs</u> ; <i>Proc. of the BCTM</i> , pp. 133-36, 1999.
	Lui et al., <u>Single Mask Metal-Insulator-Metal (MIM) Capacitor with Copper Damascene Metallization for Sub-0.18<math>\mu</math>m Mixed Mode Signal and System-on-a-Chip (SoC) Applications</u> ; <i>IEEE</i> , pp. 111-13, 2000.
	Mahnkopf et al., <u>'System on a Chip' Technology Platform for 0.18<math>\mu</math>m Digital, Mixed Signal &amp; eDRAM Applications</u> , <i>IEDM</i> , pp. 849-52, 1999.
	Bolam et al., <u>Electrical Characteristics and Reliability of UV Transparent Si<sub>3</sub>N<sub>4</sub> Metal-Insulator-Metal (MIM) Capacitors</u> , <i>IEEE Transactions on Electron Devices</i> , Vol. 50, No. 4, pp. 941-44, 2003.

EXAMINER

DATE  
CONSIDERED

EXAMINER: Initial citation considered. Draw line through citation if not in the conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449)